CLAIMS

I claim:

1. A MEMS driver, comprising:

a programmable current source, the programmable current source generating an output current for a programmable time; and

an integrator coupled to receive the output current from the programmable current source, the integrator providing a voltage which can be coupled to a drive electrode of a MEMS structure.

2. The driver of claim 1, wherein the output current increases or decreases the voltage provided by the integrator by an amount controlled by a digital control word.

3. The driver of claim 1, wherein the programmable current source is coupled to receive a digital control word including one or more bits representing the programmable time.

4. The driver of claim 3, wherein the programmable current source generates the output current in a programmable direction, the digital control word including a bit representing the programmable direction.

5. The driver of claim 4, wherein the programmable current source generates the output current at a programmable current level, the digital control word including one or more bits representing the programmable current level.

6. The driver of claim 1, wherein the MEMS structure is external to the MEMS driver.

7. The driver of claim 1, wherein the MEMS driver fits within the footprint of the MEMS structure to be driven by the MEMS driver.

8. The driver of claim 7, wherein the footprint is at most 1.2 by 1.2 mm^2.

9. The driver of claim 7, wherein the MEMS structure is a micromirror.

10. The driver of claim 1, wherein the programmable current source comprises:

a counter coupled to receive one or more bits representing the programmable time, the counter generating an active count signal during the programmable time;

a reference current source coupled to the counter to receive the active count signal, the reference current source generating a reference current while receiving the active count signal; and

an output stage coupled to the reference current source to receive the reference current, the output stage generating the output current proportional to the reference current.

11. The driver of claim 10, wherein the programmable current source further comprises a first data storage element coupled to receive a bit representing a programmable direction, the first data storage element storing the bit representing the programmable direction, the reference current source being coupled to the first data storage element to receive the bit representing the programmable direction, the reference current source generating the reference current through a path determined by the programmable direction.

12. The driver circuit of claim 11, wherein the programmable current source further comprises at least a second data storage element coupled to receive one or more bits representing a programmable current level, the second data storage element storing the one or more bits representing the programmable current level, the reference current source being coupled to the second data storage element to receive the one or more bits representing the programmable current level, thereby to cause the reference current source to generate the reference current at the programmable current level.

13. The driver circuit of claim 1, wherein the integrator is a capacitor.

14. A MEMS driver, comprising:

a programmable current source, comprising:

a reference current source coupled to receive a digital control word, the reference current source generating a reference current in response to the digital control word; and

an output stage coupled to the reference current source to receive the reference current, the output stage generating an output current proportional to the reference current;

an integrator coupled to the output stage to receive the output current, the integrator providing a voltage; and

a conductor for coupling the voltage to a drive electrode of a MEMS structure, wherein the output current increases or decreases the voltage provided by the integrator by an amount and in a direction controlled by the digital control word.

15. The MEMS driver of claim 14, wherein the digital control word is supplied by a controller external to the MEMS driver and the controller receives a feedback signal of a position of the MEMS structure.

16. The MEMS driver of claim 14, wherein the MEMS structure is external to the MEMS driver.

17. The MEMS driver of claim 14, wherein the MEMS driver fits within a footprint of the MEMS structure to be driven by the MEMS driver.

18. The MEMS driver of claim 17, wherein the footprint is at most 1.2 by 1.2 mm^2.

19. The MEMS driver of claim 17, wherein the MEMS structure is a micromirror.

20. The MEMS driver of claim 14, wherein the programmable current source further comprises:

a counter coupled to receive one or more bits representing an integration duration from the digital control word, the counter generating an active count signal during the integration duration; and

a plurality of storage elements coupled to receive a bit representing an integration direction and one or more bits representing an integration current level from the digital control word, the storage elements storing the bit representing the

integration direction and the one or more bits representing the integration current level;

wherein the reference current source is coupled to the counter to receive the active count signal, and to the storage elements to receive the bit representing the integration direction and the one or more bits representing the integration current level, and wherein the reference current source is capable of generating the reference current through a first path or a second path determined by the integration direction at the integration current level while receiving the active count signal.

21. The MEMS driver of claim 20, wherein the reference current source comprises:

a first current mirror comprising:

a reference branch; and

a plurality of output branches including a common output node; and

a decoder for selectively enabling none, one, or more of the plurality of output branches of the first current mirror to generate an internal reference current on the common output node.

22. The MEMS driver of claim 21, wherein the first current mirror further comprises a transistor coupling the reference branch to ground, the transistor including a gate terminal coupled to a reference bias voltage.

23. The MEMS driver of claim 21, wherein the first current mirror is a PMOS cascode current mirror.

24. The MEMS driver of claim 21, wherein the plurality of output branches comprises four output branches having current mirror ratios of 1:1, 1:1, 2:1, and 4:1 to the reference branch of the first current mirror.

25. The MEMS driver of claim 21, wherein:

the first current mirror further comprises a plurality of switches each coupling an output branch to a common voltage supply; and

the decoder comprises a plurality of logic gates including:

input lines coupled to the counter and at least one of the plurality of storage elements to respectively receive the active count signal and the one or more bits representing the integration current level; and

output terminals coupled to gate terminals of the switches.

26. The MEMS driver of claim 21, wherein the reference current source further comprises a second current mirror, the second current mirror comprising:

a reference branch coupled to the common output node of the first current mirror to receive the internal reference current; and

a first plurality of output branches including the first common output node;

wherein the decoder selectively enables none, one or more of the first plurality of output branches of the second current mirror to generate the reference current on the first common output node.

27. The MEMS driver of claim 26, wherein the second current mirror is a cascode current mirror.

28. The MEMS driver of claim 26, wherein the second current mirror is a NMOS current mirror.

29. The MEMS driver of claim 26, wherein the first plurality of mirror branches comprises two output branches having current mirror ratios of 15:4 and 1:4 to the reference branch of the second current mirror.

30. The MEMS driver of claim 26, wherein:

the second current mirror further comprises a plurality of switches each coupling an output branch of the first plurality of output branches to a common voltage supply; and

the decoder comprises a plurality of logic gates including:

input lines coupled to the counter to receive the active count signal and to the plurality of storage elements to receive the bit representing the integration direction and the one or more bits representing the integration current level; and

output terminals coupled to gate terminals of the switches.

31. The MEMS driver of claim 26, wherein the second current mirror further comprises a second plurality of output branches including the second common output node, and wherein the decoder selectively enables one or more of the second plurality of output branches of the second current mirror to generate the reference current on the second common output node.

32. The MEMS driver of claim 31, wherein the second current mirror is a NMOS cascode current mirror.

33. The MEMS driver of claim 31, wherein the second plurality of mirror branches comprises two output branches having current mirror ratios of 15:4 and 1:4 to the reference branch of the second current mirror.

34. The MEMS driver of claim 31, wherein:

the second current mirror further comprises a plurality of switches each coupling an output branch from the first and the second pluralities of output branches to a common voltage supply; and

the decoder comprises a plurality of logic gates including:

input lines coupled to the counter to receive the active count signal and to the plurality of storage elements to receive the bit representing the integration direction and one or more bits representing the integration current level; and

output terminals coupled to gate terminals of the switches.

35. The MEMS driver of claim 31, wherein the output stage comprises:

a first current mirror, comprising:

a first reference branch coupled to the first common output node of the second current mirror of the reference current source to receive the reference current; and

a first output branch including a first output node;

a second current mirror, comprising:

a second reference branch coupled to the first output node of the first mirror branch; and

a second output branch including a second output node coupled to the integrator, the second output node carrying the output current in a down direction.

36. The MEMS driver of claim 35, wherein at least one of the first and the second current mirrors is a NMOS cascode current mirror.

37. The MEMS driver of claim 35, wherein the first and the second output branches have respective current mirror ratios of 1:4 and 1:1 to the first and the second reference branches.

38. The MEMS driver of claim 35, wherein the second output branch includes a high voltage transistor.

39. The MEMS driver of claim 35, wherein the output stage further includes a transistor coupling the first reference branch to ground, the transistor including a gate terminal coupled to the reference bias voltage.

40. The MEMS driver of claim 35, wherein the output stage further comprises:

a third current mirror, comprising:

a third reference branch coupled to the second common output node of the second current mirror of the reference current source to receive the reference current; and

a third output branch including a third output node;

a fourth current mirror, comprising:

a fourth reference branch coupled to the third output node of the third output branch; and

a fourth output branch including a fourth output node;

a fifth current mirror, comprising:

a fifth reference branch coupled to the fourth output node of the fourth output branch; and

a fifth output branch including a fifth output node coupled to the integrator, the fifth output node carrying the output current in an up direction.

41. The MEMS driver of claim 40, wherein the third and the fifth current mirrors are PMOS cascode current mirrors.

42. The MEMS driver of claim 40, wherein the third, the fourth, and the fifth output branches have current mirror ratios of 1:4, 1:1, and 1:1 to the third, the fourth, and the fifth reference branches.

43. The MEMS driver of claim 40, wherein each of the fourth and the fifth output branches includes a high voltage transistor including a source coupled to a high voltage supply.

44. The MEMS driver of claim 40, wherein the output stage further includes a transistor coupling the third reference branch to ground, the transistor including a gate terminal coupled to the bias voltage.

45. The MEMS driver of claim 14, wherein the integrator is a capacitor.

46. A driver circuit for electrostatically driving a MEMS structure, comprising:

a programmable current means generating an output current for a programmable time; and

an integrating means coupled to receive the output current from the programmable current means, the integrating means providing a voltage which can be coupled to a drive electrode of a MEMS structure.

47. The driver circuit of claim 46, wherein the output current increases or decreases the voltage provided by the integrating means by an amount controlled by a digital control word.

48. The driver circuit of claim 46, wherein the programmable current means is coupled to receive a digital control word including one or more bits representing the programmable time.

49. The driver circuit of claim 48, wherein the programmable current means generates the output current in a programmable direction, the digital control word including a bit representing the programmable direction.

50. The driver circuit of claim 49, wherein the programmable current means generates the output current at a programmable current level, the digital control word including one or more bits representing the programmable current level.

51. The driver circuit of claim 46, wherein the MEMS structure is external to the driver circuit.

52. The driver circuit of claim 46, wherein the driver circuit fits within a footprint of the MEMS structure to be driven by the driver circuit.

53. The driver circuit of claim 52, wherein the MEMS structure is a micromirror.

54. The driver circuit of claim 52, wherein the programmable current means comprises:

a timing means coupled to receive one or more bits representing the programmable time, the timing means generating an active count signal during the programmable time; and

a reference current means coupled to the timing means to receive the active count signal, the reference current means generating a reference current while receiving the active count signal; and

a voltage output means coupled to the reference current means to receive the reference current, the voltage output means generating the output current proportional to the reference current.

55. The driver circuit of claim 54, wherein the programmable current means further comprises a first data storage means coupled to receive a bit representing a programmable direction, the first data storage means storing the bit representing the programmable direction, the reference current means being coupled to the first data storage means to receive the bit representing the programmable direction, the reference current means generating the reference current through a path determined by the programmable direction.

56. The driver circuit of claim 55, wherein the programmable current means further comprises at least a second data storage means coupled to receive one or more bits representing a programmable current level, the second data storage means storing the one or more bits representing the programmable current level, the reference current means being coupled to the second data storage means to receive the one or more bits representing the programmable current level, the reference current means generating the reference current at the programmable current level.

57. A method for operating a driver circuit electrostatically driving a MEMS structure, comprising:

generating a first output current in response to a first digital control word; and

integrating the first output current to increase or decrease a first voltage by an amount and in a direction controlled by the first digital control word to obtain a

second voltage which can be coupled to a drive electrode that electrostatically drives the MEMS structure.

58. The method of claim 57, wherein the driver circuit fits within a footprint of the MEMS structure to be driven by the driver circuit.

59. The method of claim 58, wherein the footprint is at most 1.2 by 1.2 mm^2.

60. The method of claim 58, wherein the MEMS structure is a micromirror.

61. The method of claim 57, wherein the first digital control word includes one or more bits representing an integration duration and said generating the first output current comprises generating the first output current for the integration duration.

62. The method of claim 61, wherein the first digital control word further includes a bit representing an integration direction and said generating the first output current further comprises generating the first output current in the integration direction.

63. The method of claim 62, wherein the first digital control word further includes one or more bits representing an integration current level and said generating the first output current further comprises generating the first output current at the integration current level.

64. The method of claim 57, further comprising:

generating a second output current in response to a second digital control word;

integrating the second output current to increase or decrease the second voltage by an amount and in a direction controlled by the second digital control word to obtain a third voltage which can be coupled to the drive electrode.

65. A method for operating a driver circuit that electrostatically drives a MEMS structure, comprising:

receiving a first digital control word including information relating to a first integration duration, a first integration direction, and a first integration

current level, the first digital control word representing a change to a first voltage across an integrate-and-hold capacitor;

in response to the first digital control word, generating a first reference current in the first integration direction, at the first integration current level, and for the first integration duration; and

in response to the first reference current, generating a first output current in the first integration direction, at a level scaled relative to the first integration current level, and for the first integration duration;

supplying the first output current to the integrate-and-hold capacitor, wherein a second voltage develops across the integrate-and-hold capacitor and can be coupled to a drive electrode that electrostatically drives the MEMS structure.

66. The method of claim 65, wherein the driver circuit fits within a footprint of the MEMS structure to be driven by the driver circuit.

67. The method of claim 66, wherein the structure is a micromirror.

68. The method of claim 66, further comprising:

receiving a second digital control word including information relating to a second integration duration, a second integration direction, and a second integration current level, the second digital code word representing a change to the second voltage across the integrate-and-hold capacitor;

in response to the second digital control word, generating a second reference current in the second integration direction, at the second integration current level, and for the second integration duration;

in response to the second reference current, generating a second output current in the second integration direction, at a level scaled relative to the second integration current level, and for the second integration duration; and

supplying the second output current to the integrate-and-hold capacitor, wherein a third voltage develops across the integrate-and-hold capacitor and can be coupled to the drive electrode.

69. The method of claim 65, wherein said generating the first output reference current comprises:

in response to receiving the information relating to the first integration duration, generating an active count signal during the first integration duration;

in response to receiving the active count signal and the information relating to the first integration current level, enabling a combination of output branches in a first current mirror to generate an internal reference current;

in response to receiving the active count signal and the information relating to the integration direction, allowing the enabling of a first plurality of output branches or a second plurality of output branches in a second current mirror, the second current mirror including a reference branch receiving the internal reference current; and

in response to receiving the information relating to the first integration current level, enabling a combination of the output branches of the first or the second plurality of output branches allowed by the active count signal and the information relating to the integration direction to generate the output reference current.

70. The method of claim 65, wherein said generating the first output current comprises:

supplying the first reference current to a first current mirror, wherein the first current mirror generates an internal reference current scaled relative to the first reference current; and

supplying the internal reference current to a second current mirror, wherein the second current mirror generates the first output current in a down direction scaled relative to the internal reference current.

71. The method of claim 70, wherein the second current mirror comprises an output branch including a high voltage transistor comprising a source coupled to a high voltage supply.

72. The method of claim 70, further comprising supplying a small current to the first current mirror when the reference current is zero.

73. The method of claim 65, wherein said generating the first output current comprises:

supplying the first reference current to a third current mirror, wherein the third current mirror generates a third internal reference current scaled relative to the first reference current;

supplying the first internal reference current to a fourth current mirror, wherein the fourth current mirror generates a fourth internal reference current scaled relative to the first internal reference current; and

supplying the fourth reference current to a fifth current mirror, wherein the fifth current mirror generates the first output current in an up direction scaled relative to the fourth internal reference current.

74. The method of claim 73, wherein each of the fourth and the fifth current mirrors comprises an output branch including a high voltage transistor having a source coupled to a high voltage supply.

75. The method of claim 73, further comprising supplying a small current to the third current mirror when the reference current is zero.